RELAY CONTROL CHART

CONTROL	CODE	DEVICE	FUNCTION	CONNECTOR

JUMPER TABLE

JP#	ON	OFF
1		
2		
3		
4		
5		

* SEE ASSEMBLY INSTRUCTIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	RELEASED	22JUN15	B H
B	PARTS CHANGES DNI	22AUG15	B H
C	CHANGES TO BALUM	05NOV15	B H

DECEMBER 8 2015

P.O SPEC.	BK/BD SPEC.	SOCKET OEM	OEM PART#	HANDLER

TEMPLATE ENGINEER P.ALONGI	DATE
HARDWARE SERVICES -	
HARDWARE SYSTEMS -	
TEST ENGINEER -	
COMPONENT ENGINEER -	
TEST PROCESS -	
HARDWARE RELEASE -	
DESIGNER -	
PTD ENGINEER <PTD_ENGINEER>	
CHECKER -	

SCHEMATIC

ANALOG DEVICES

AD9162 BRD
<PRODUCT>
<PRODUCT_1>
<DRAWING_TITLE1>
<DRAWING_TITLE2>
<DRAWING_TITLE3>
<DRAWING_TITLE4>
<DRAWING_TITLE5>

MASTER PROJECT TEMPLATE: <DRAWING_TITLE6>
TESTER TEMPLATE: -

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES

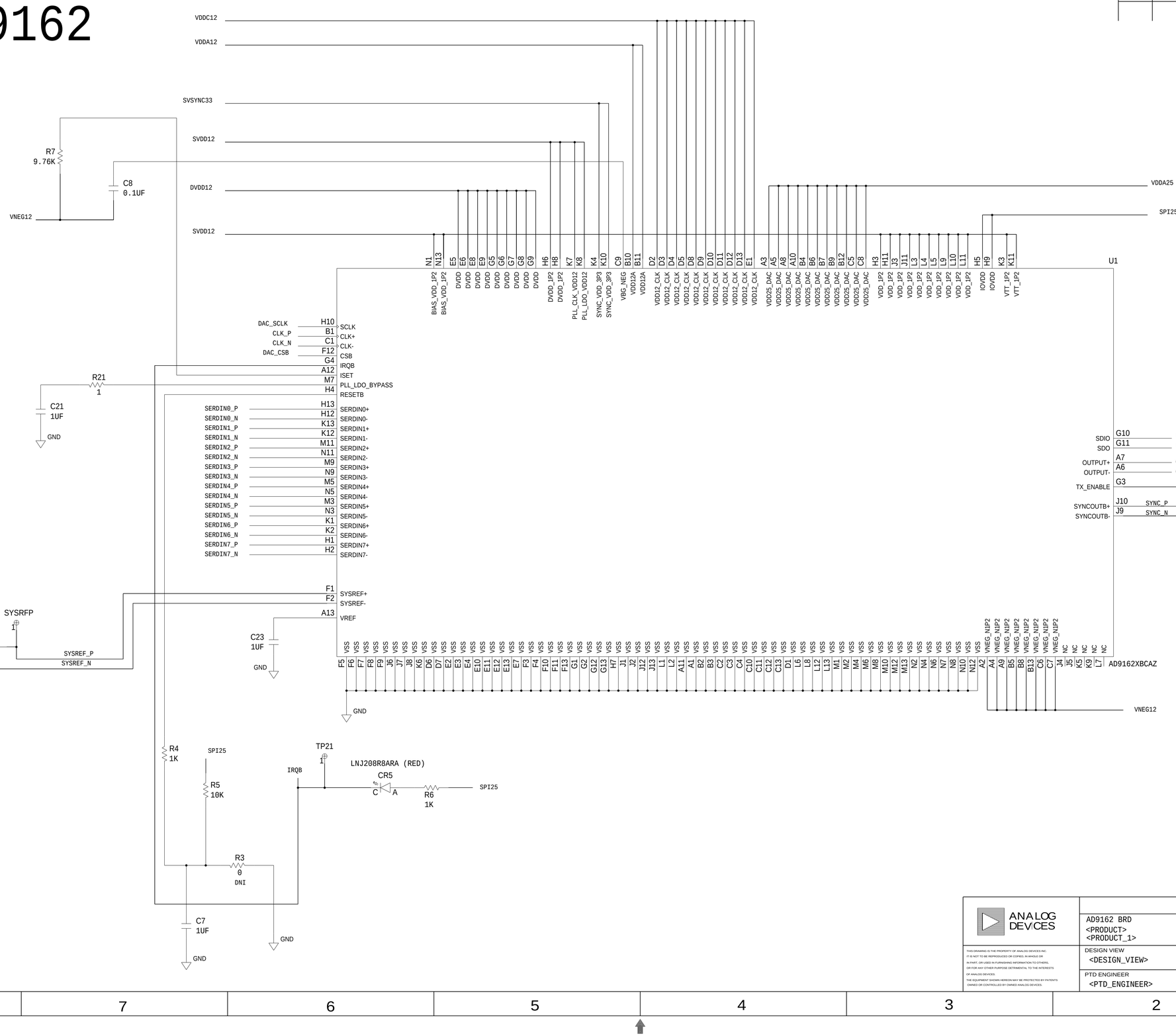
DECIMALS	FRACTIONS	ANGLES
X.XX +-0.010 X.XXX +-0.005	+-1/32	+-2

DRAWING NO. HSC 15017
REV. C

SIZE D | SCALE <SCALE>- | CODE ID NO. | SHEET 1 OF 8

AD9162

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES	SCHEMATIC		
	AD9162 BRD <PRODUCT> <PRODUCT_1>		
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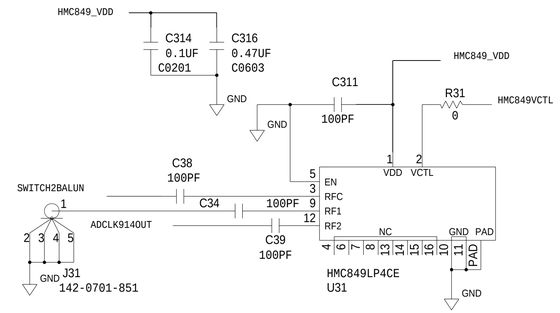
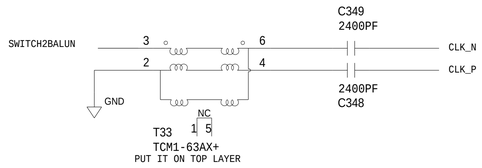
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
			SHEET 2 OF 8

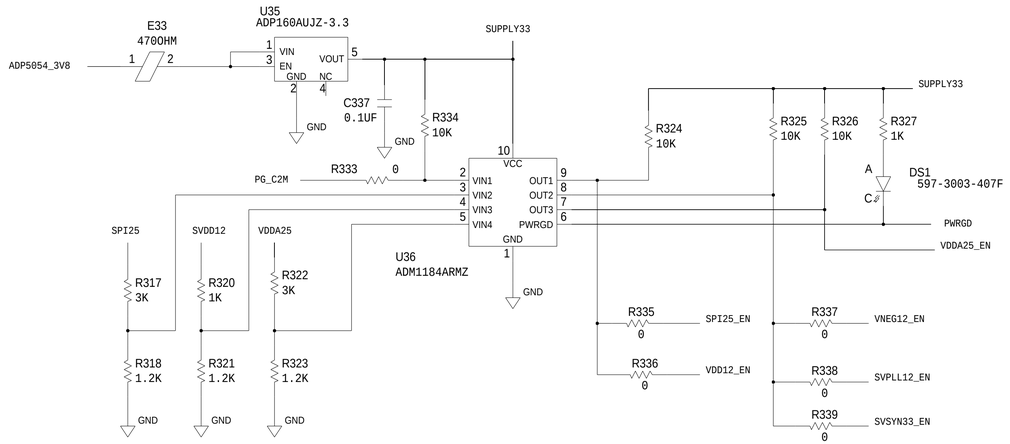
DAC OUTPUT & CLK & POWER SEQUENCE

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

REF CLK







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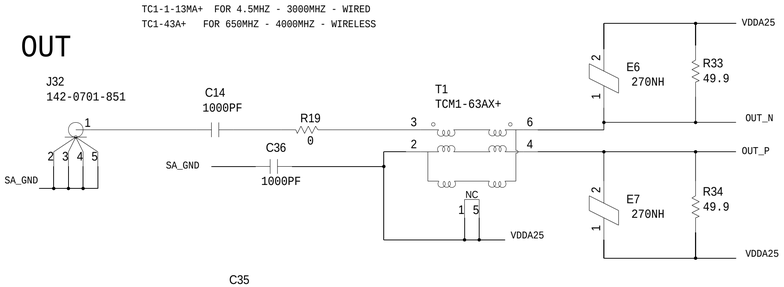
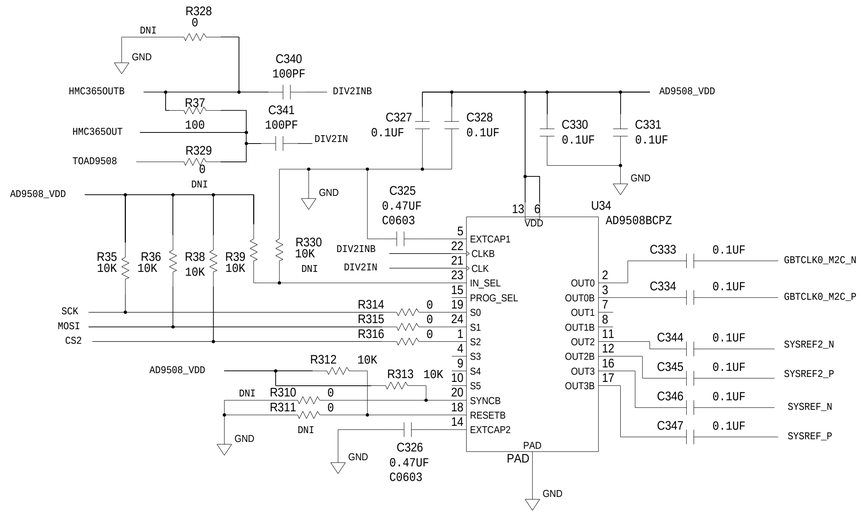
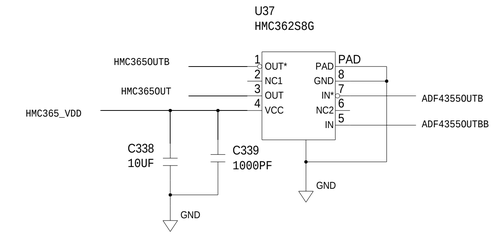
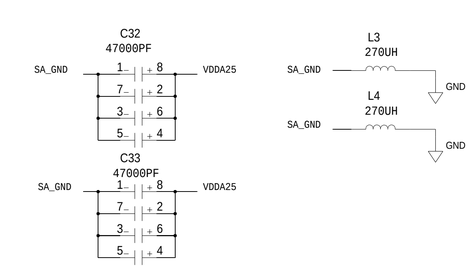
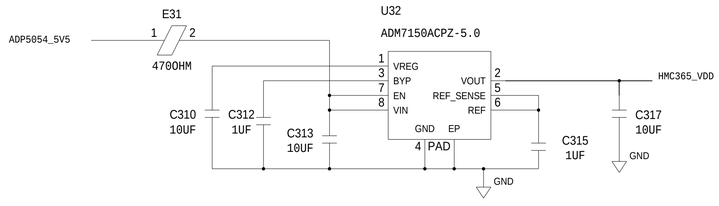
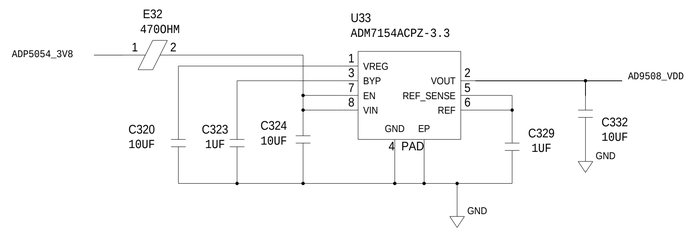












ANALOG DEVICES

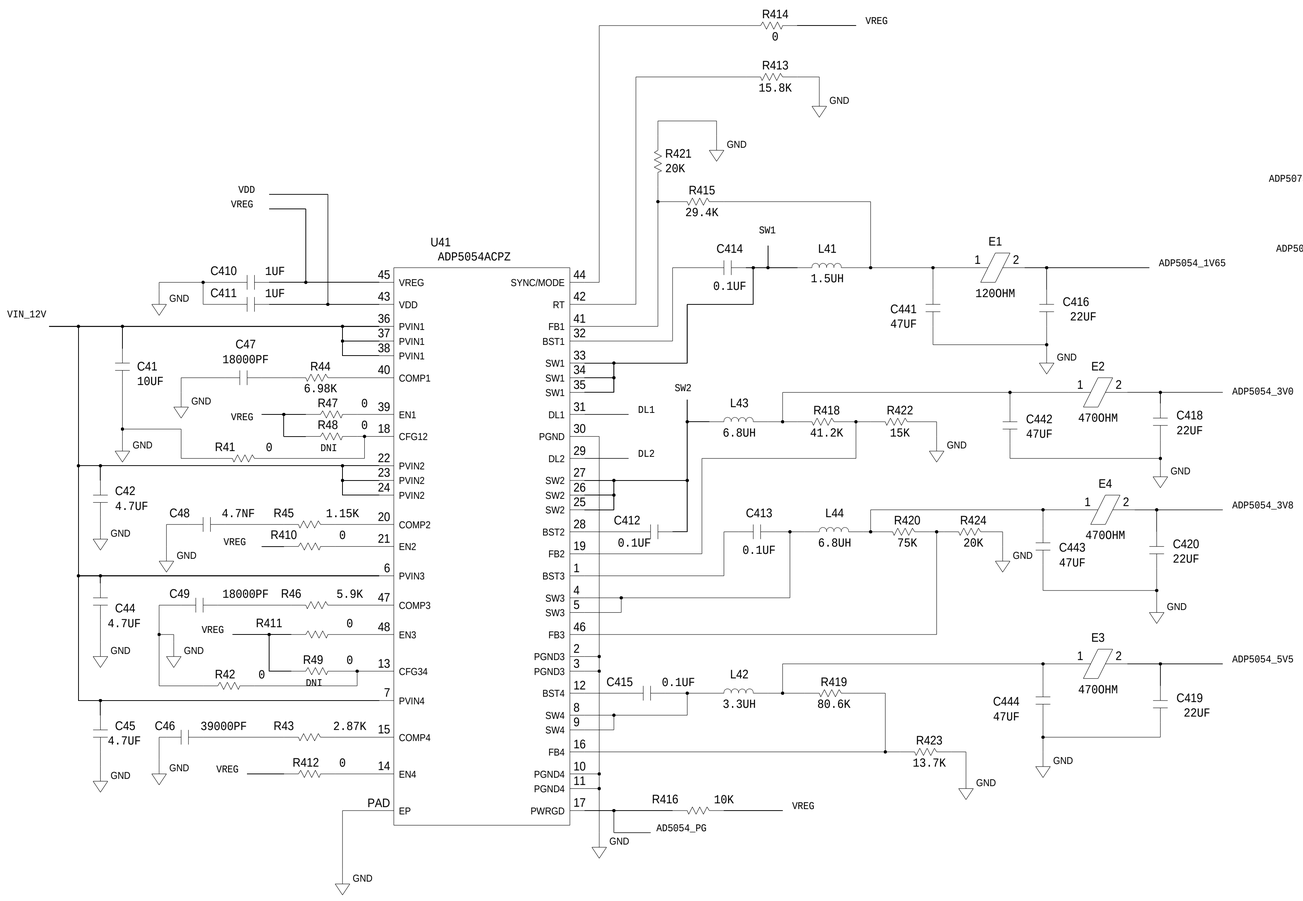
SCHEMATIC

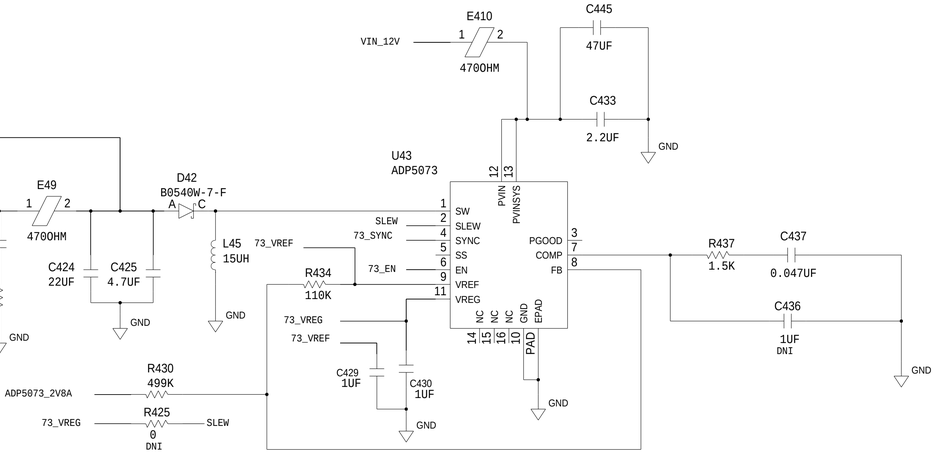
<PRODUCT_1> AD9162 BRD

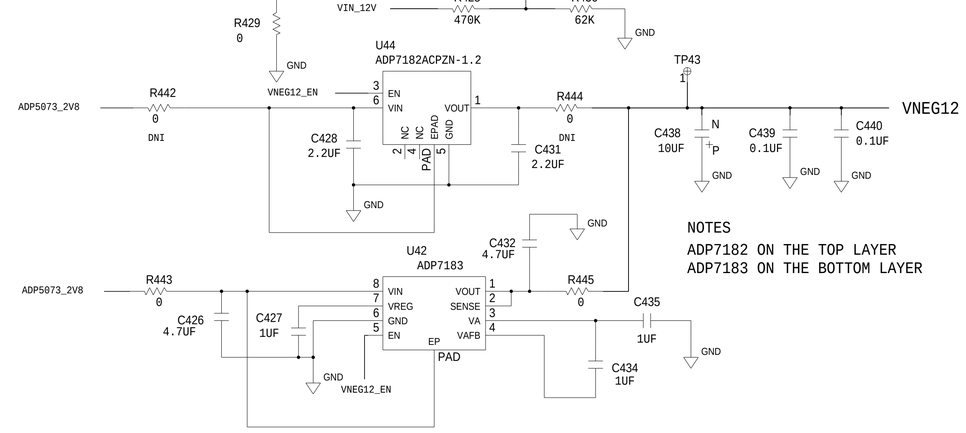
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 15017	REV C
PTD ENGINEER <PTD_ENGINEER>	SIZE D / SCALE <SCALE>	SHEET 3 OF 8

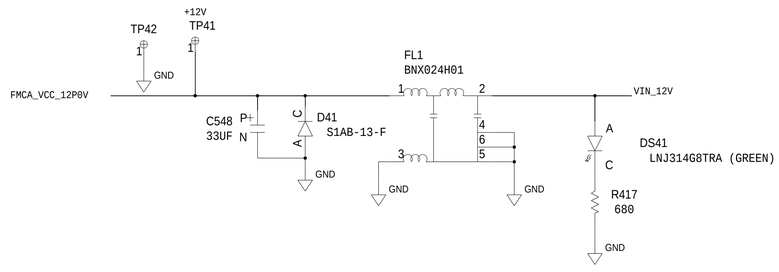
POWER - REGULATOR & NEG LDO

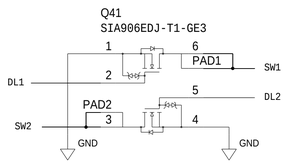
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED











ANALOG DEVICES

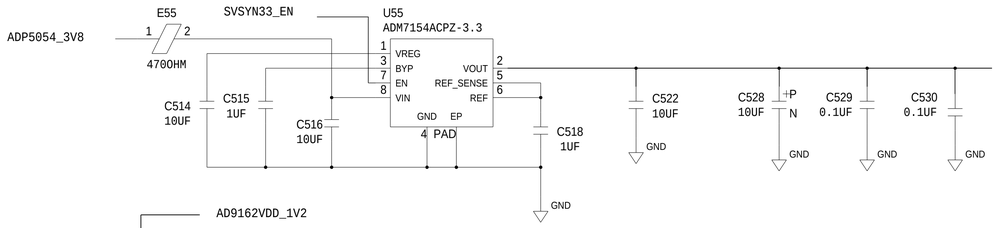
SCHEMATIC

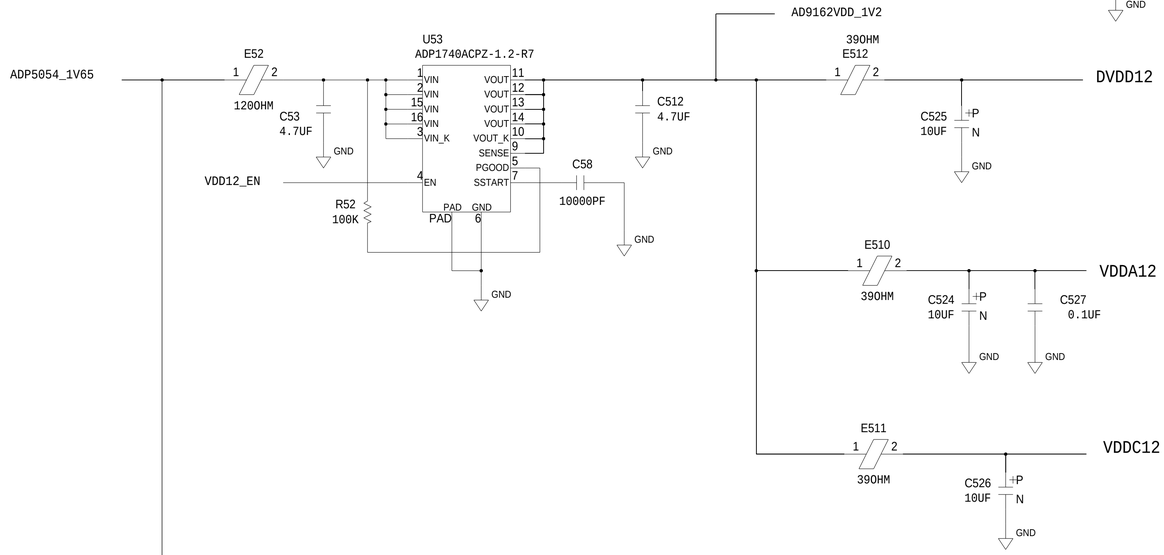
AD9162 BRD
<PRODUCT>
<PRODUCT_1>

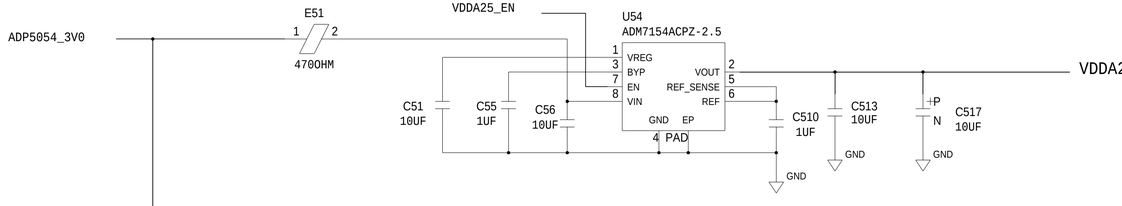
DESIGN VIEW	DRAWING NO.	REV
<DESIGN_VIEW>	HSC 15017	C
PTD ENGINEER	SIZE / SCALE	SHEET 4 OF 8
<PTD_ENGINEER>	D / <SCALE>	

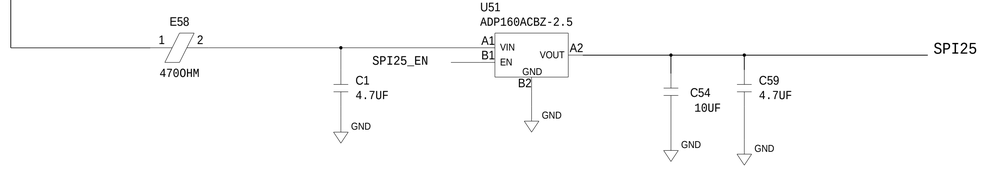
POWER - LDO

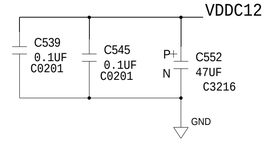
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

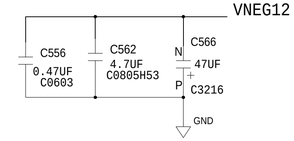


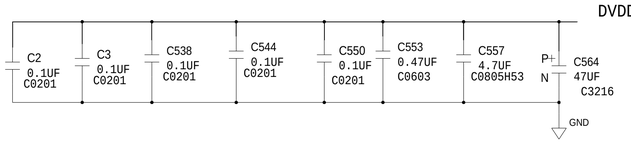


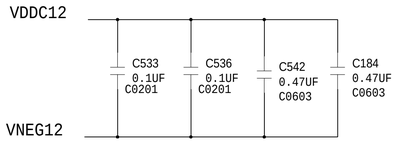


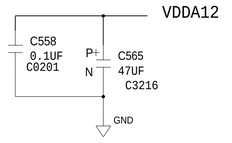


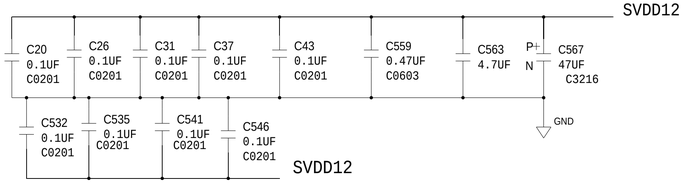












ANALOG DEVICES	SCHEMATIC	
	AD9162 BRD <PRODUCT> <PRODUCT_1>	
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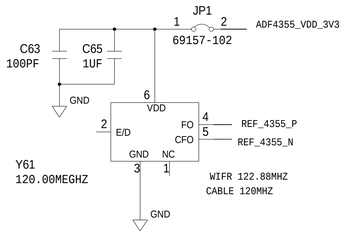
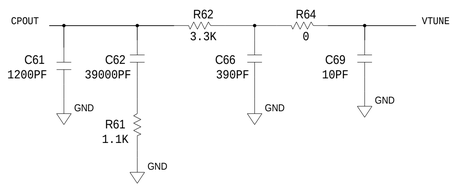
	PTD ENGINEER: <PTD_ENGINEER>	SIZE: D — SCALE: <SCALE> — SHEET 5 OF 8

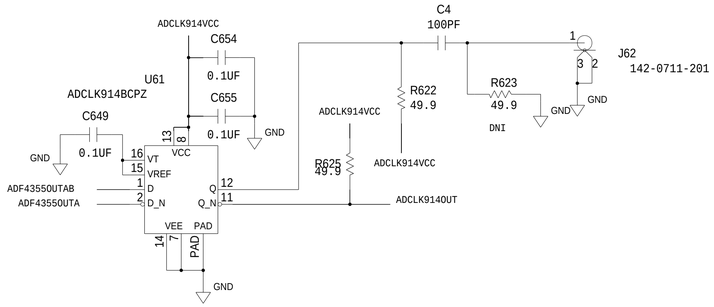
ONBOARD CLK - ADF4355 & CLK BUFFER

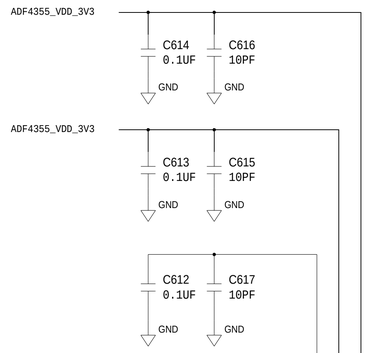
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

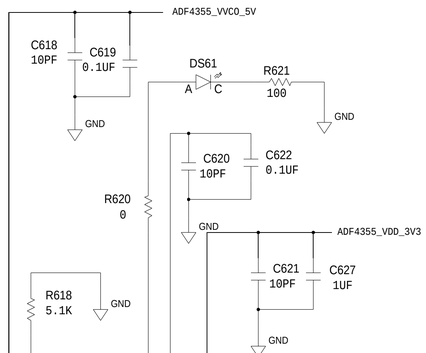


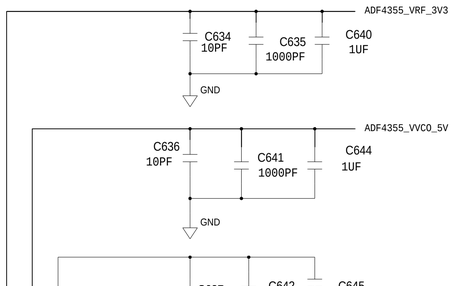
NOTES
PLACE ON THE BOTTOM SIDE
SHIELD SIGNALS WITH VIAS

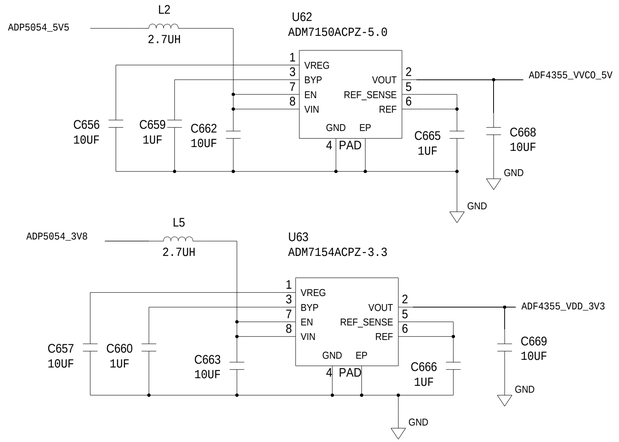


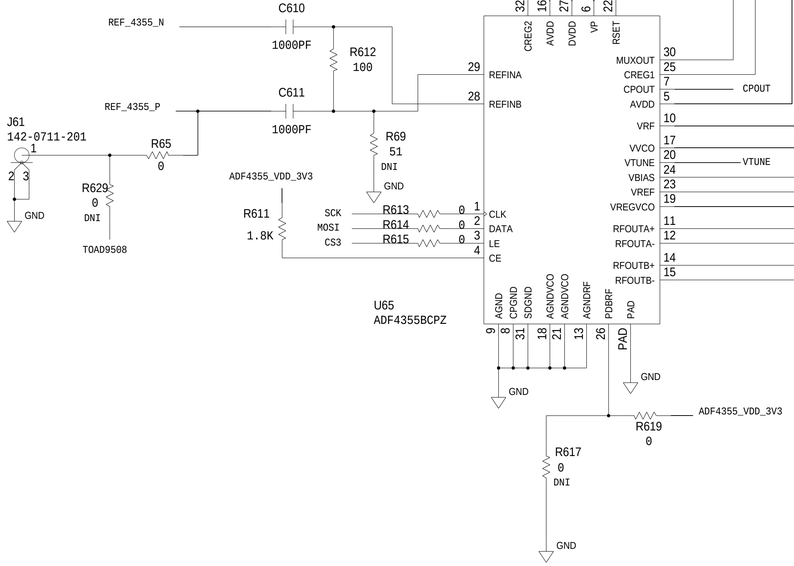


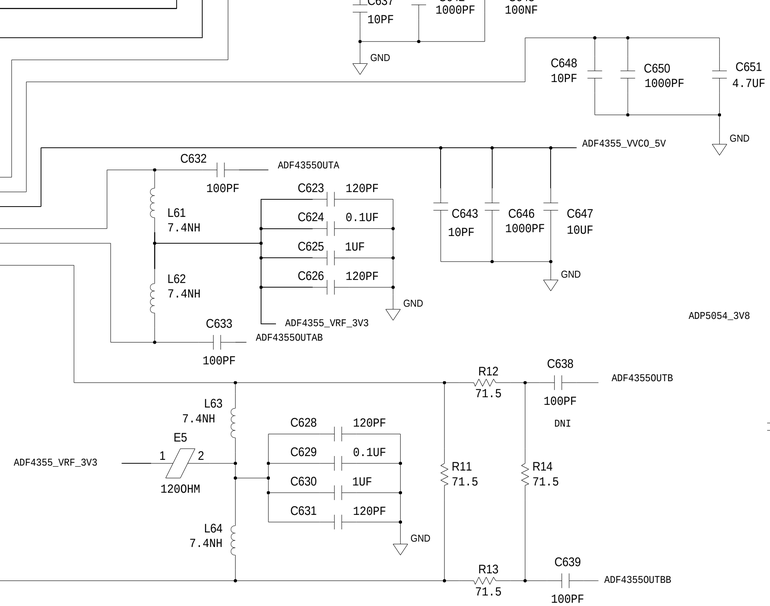


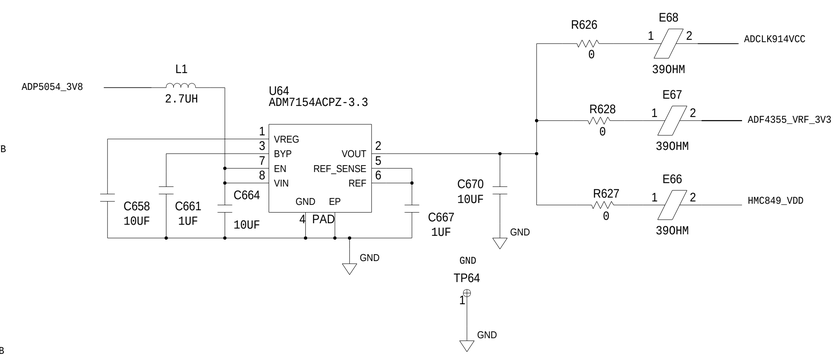










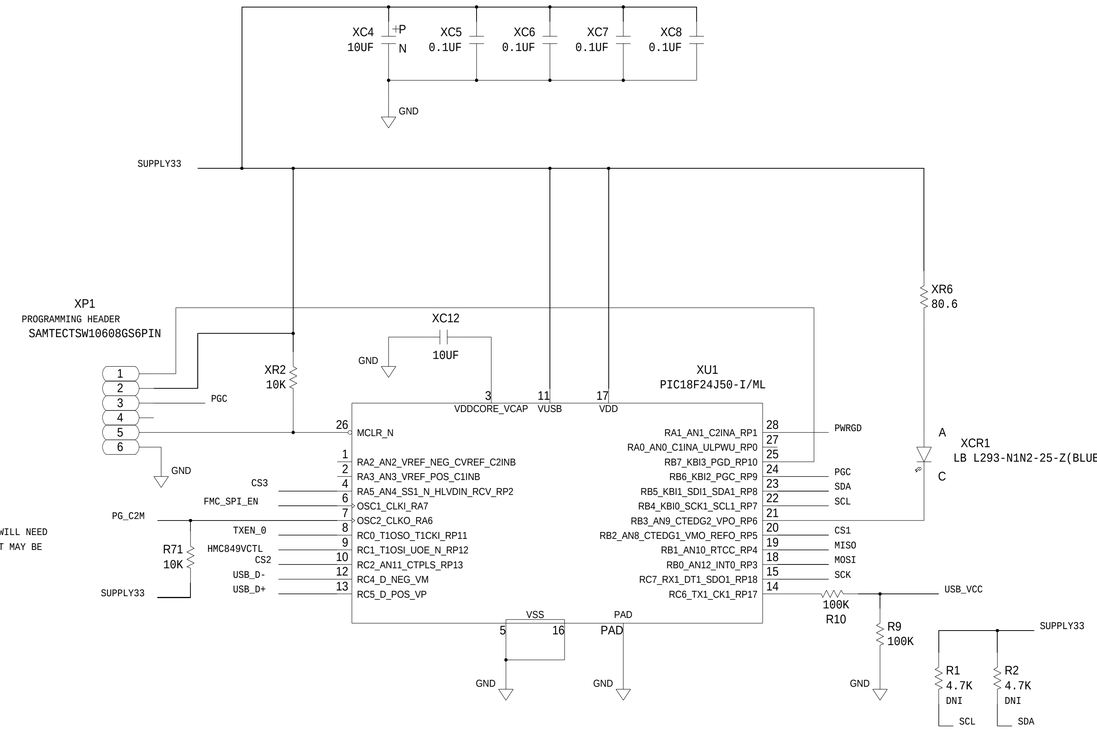


L0 (ADF4355)

ANALOG DEVICES	SCHEMATIC
	AD9162 BRD <PRODUCT> <PRODUCT_1>
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. HSC 15017 — REV C
PTD ENGINEER <PTD_ENGINEER>	SIZE D — SCALE <SCALE> — SHEET 6 OF 8

GPIO & MISC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

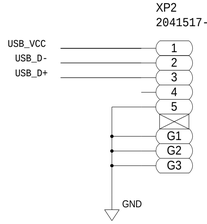


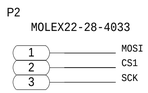
IMPLEMENTATION NOTE: FMC_SPI_EN WILL NEED TO BE SAMPLED AS ANALOG, SINCE IT MAY BE AS LOW AS 1.2V LOGIC HIGH.

NOTE:

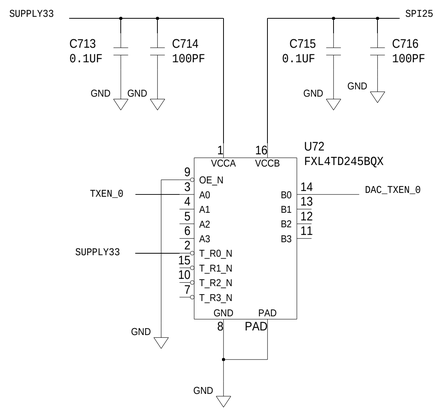
IF USB CABLE IS PLUGGED IN PIC IS THE SOURCE OF SPI BUS AND TXEN SIGNALS

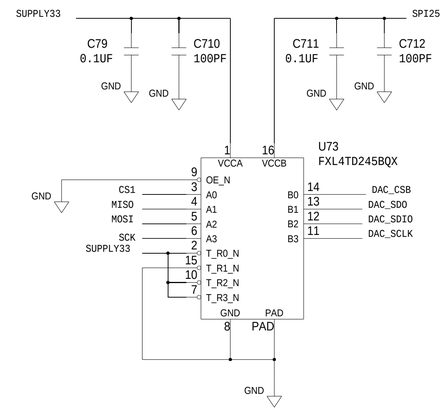
IF USB IS UNPLUGGED FMC INTERFACE IS THE SOURCE OF SPI BUS AND TXEN SIGNAL.

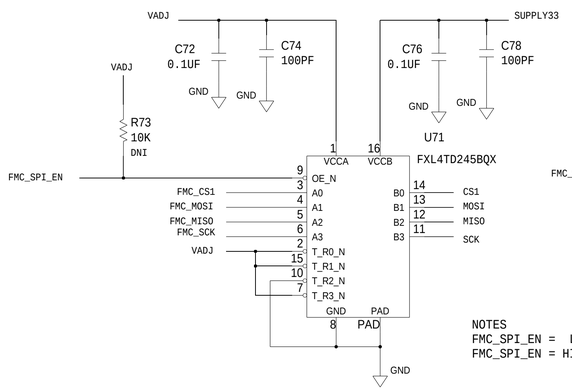




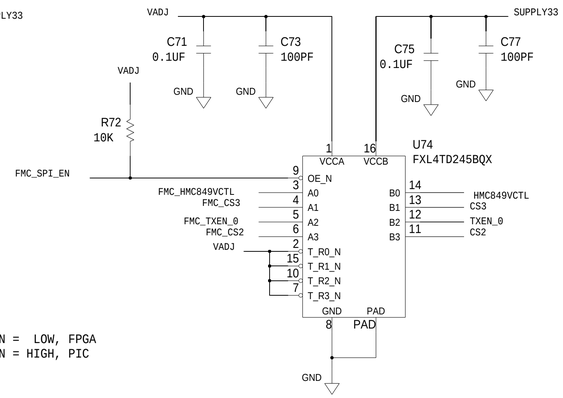
CONNECTIONS WILL PASS RIGHT THROUGH THE CONNECTOR







NOTES
FMC_SPI_EN = LOW, FPGA
FMC_SPI_EN = HIGH, PIC



ANALOG DEVICES	SCHEMATIC	
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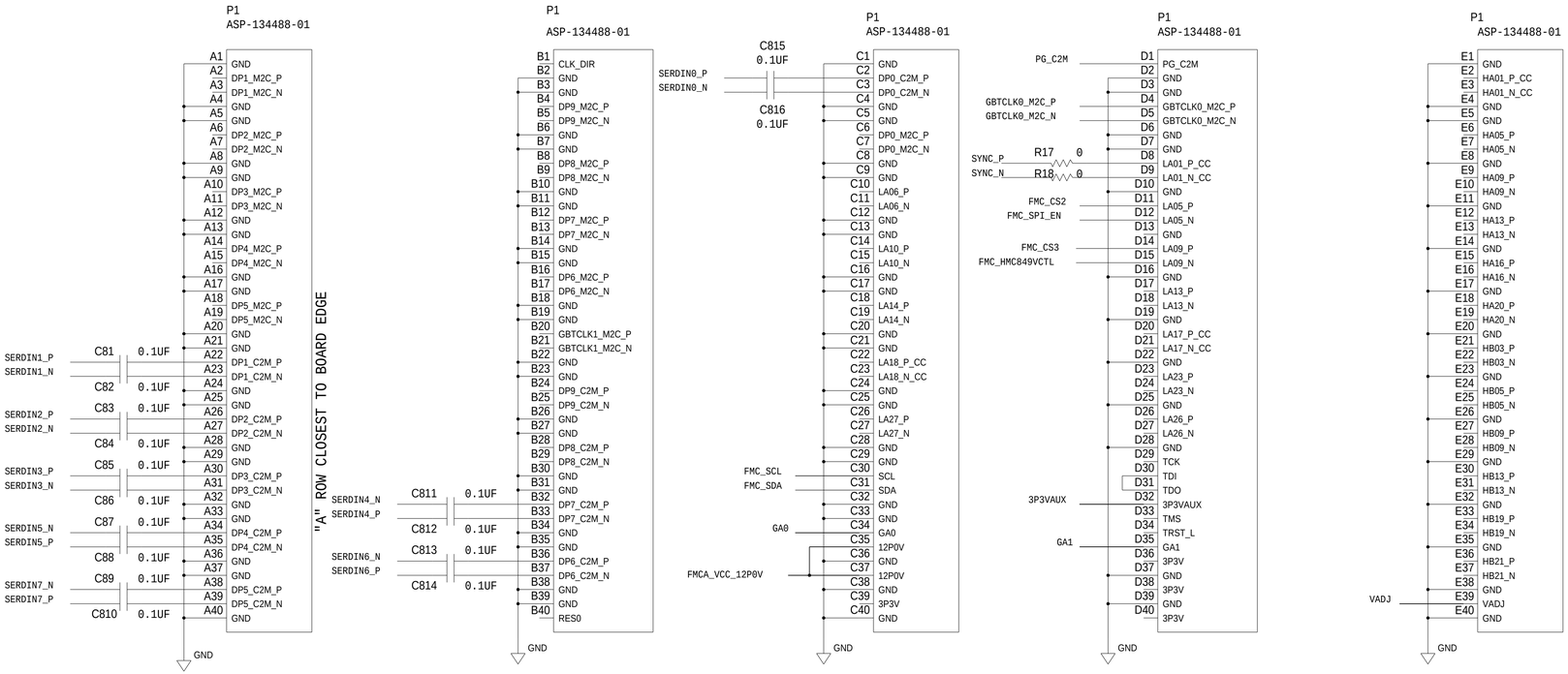
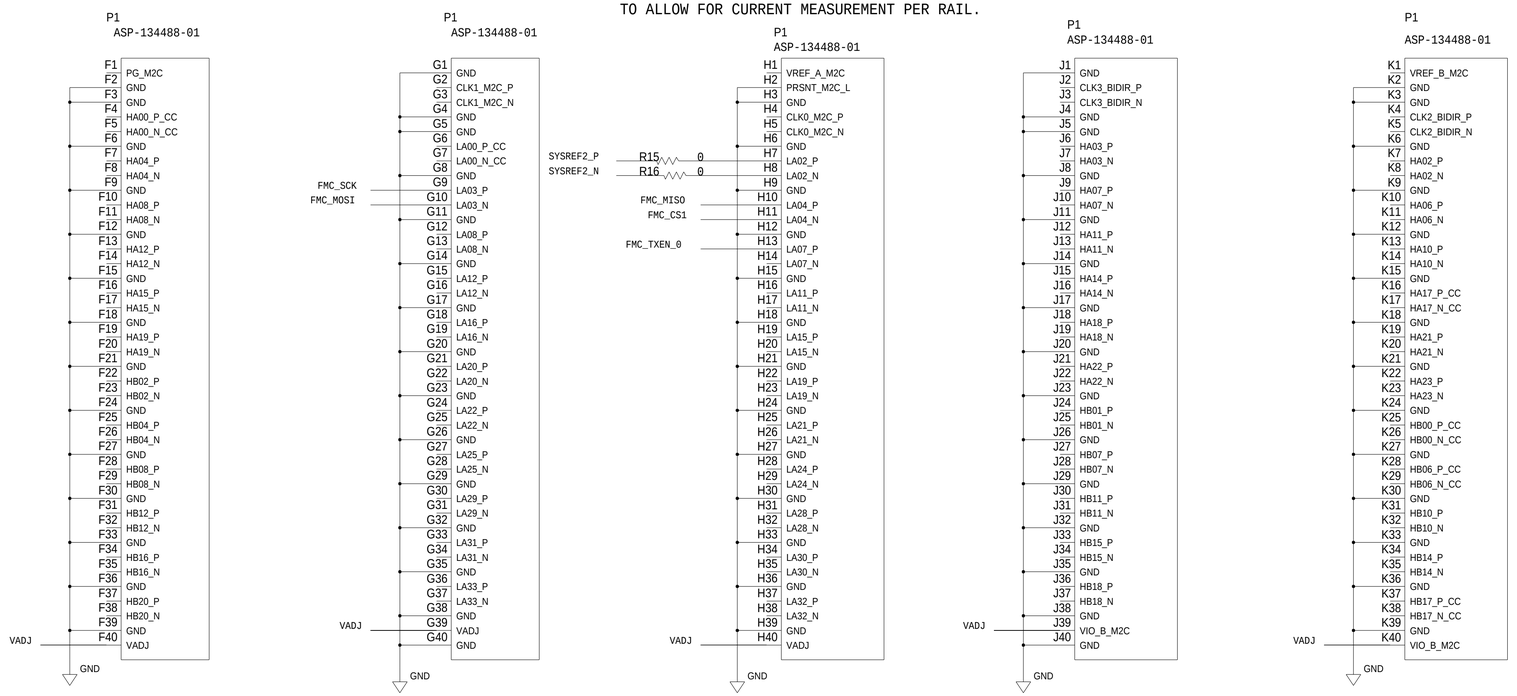
	DESIGN VIEW: <DESIGN_VIEW>	DRAWING NO.: HSC 15017 — REV: C
	PTD ENGINEER: <PTD_ENGINEER>	SIZE: D — SCALE: <SCALE> — SHEET 7 OF 8

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

FMC - CONNECTIONS

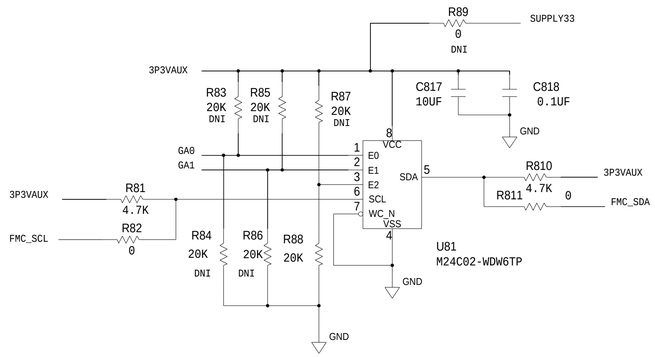


ON 3P3V, 12P0V, AND VADJ, HAVE PIN-HEADER JUMPER BETWEEN FMC PINS AND REST OF BOARD, TO ALLOW FOR CURRENT MEASUREMENT PER RAIL.



VIO_B_M2C PINS SHOULD HAVE WIDE ETCH CONNECTION TO VADJ PINS

BOARD ID EPROM



ANALOG DEVICES	SCHEMATIC		
	AD9162 BRD <PRODUCT> <PRODUCT_1>		
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	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 8 OF 8	